REMARKS

Claims 1-7 and 48-85 are now pending in the application. While Applicants disagree with the current rejections, Applicants have amended the claims to expedite prosecution. Applicants reserve the right to pursue the claims as originally filed in one or more continuing applications. Support for the amendments can be found throughout the written description, claims, and drawings as originally filed. Therefore, no new matter has been added. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 1, 3-6, 48-50, 52, 54-57, 59-61, 63, 65-71, 73-79, and 81-85 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,662,253 ("Gary"). This rejection is respectfully traversed.

Claim 63 recites that the first rate and the second rate are different, and that the servo controller interface is connected between the servo controller and the first and second processors.

A. Gary does not show, teach, or suggest that the first rate and the second rate are different, and that the servo controller interface is connected between the servo controller and the first and second processors.

The Examiner states that Gary discloses first and second processors P0 and P1 that inherently operate at respective rates, "even if that rate is the same rate." (See Page 2 of the Office Action mailed July 2, 2009, hereinafter "the Office Action"). Applicants respectfully submit that claim 63 recites that the first rate and the second rate are different. In contrast, Gary is absent of any teaching or suggestion that the processors P0 and P1 operate at first and second rates that are different.

Further, the Examiner relies on FIG. 1 of Gary to disclose buffer memory 104, which purportedly corresponds to a component of a servo controller interface because Applicants' "supplied definition (of a servo controller interface) is not specifically claimed." Claim 63 now recites that the servo controller interface is connected between the servo controller and the first and second processors. Gary appears to be absent of any teach or suggestion that the relied upon buffer 104 is connected between servo control 108 and the processors P0 and P1. Instead, the buffer 104 is located external to controller 103 and only communicates with the processors P0 and P1 via memory control 109.

The Court of Appeals for the Federal Circuit has recently stated: "We thus hold that unless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. §102… [D]ifferences between the prior art reference and a claimed invention, however slight, invoke the question of obviousness, not anticipation." *Net MoneyIN Inc. v. VeriSign Inc.*, 88 USPQ2d 1751, 1759-1760 (Fed. Cir. 2008).

Therefore, claim 63 is allowable for at least these reasons.

B. Other Claims

Independent claims 1, 52, 71, and 79 are allowable for at least similar reasons as claim 63. Dependent claims 3-6, 48-50, 54-57, 59-61, 65-70, 73-78, and 81-85 ultimately depend from claims 1, 52, 63, 71, and 79 and are therefore allowable for at least similar reasons. Applicants' position with respect to claims 3-6, 48-50, 54-57, 59-61, 65-70, 73-78, and 81-85 should not be understood as implying that no other reasons for the patentability of claims 3-6, 48-50, 54-57, 59-61, 65-70, 73-78, and 81-85 exist. Applicants reserve the right to address these other reasons at a later date if needed.

REJECTION UNDER 35 U.S.C. § 103

Claims 2, 53, 64, 72, and 80 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gary. Claims 7, 51, 58, and 62 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gary in view of U.S. Pat. No. 6,745,274 ("Snyder"). These rejections are respectfully traversed.

Snyder does not remedy the deficiencies of Gary with respect to claims 1, 52, 63, 71, and 79. Claims 2, 7, 51, 53, 58, 62, 64, 72, and 80 ultimately depend from claims 1, 52, 63, 71, and 79 and are therefore in condition for allowance for at least similar reasons. Applicants' position with respect to claims 2, 7, 51, 53, 58, 62, 64, 72, and 80 should not be understood as implying that no other reasons for the patentability of claims 2, 7, 51, 53, 58, 62, 64, 72, and 80 exist. Applicants reserve the right to address these other reasons at a later date if needed.

Further, Applicants traverse the Examiner's taking of Official Notice with respect to claims 2, 53, 64, 72, and 80. In particular, Applicants respectfully submit that communicating with processors having different rates using interfaces that are part of the same servo controller interface would not be obvious merely in view of the fact that "processors may operate at different frequencies."

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly addressed. For all of the reasons set forth above, Applicants submit that the application is in condition for allowance. Applicants therefore respectfully request that the Examiner reconsider and withdraw all presently outstanding rejections. By addressing particular positions taken by the Examiner in the above remarks, Applicants do not acquiesce to other positions that have not been explicitly addressed. In addition, Applicants' arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

If the Examiner believes that personal communication will allow any outstanding issues to be resolved, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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